Dual 256-Position I²C Compatible Digital Potentiometer

AD5243/AD5248

FEATURES

- 2-channel, 256-position
- End-to-end resistance: 2.5 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ
- Compact MSOP-10 (3 mm × 4.9 mm) package
- Fast settling time: t_S = 5 µs typ on power-up
- Full read/write of wiper register
- Power-on preset to midscale
- Extra package address decode pins AD0 and AD1 (AD5248 only)
- Computer software replaces µC in factory programming applications
- Single supply: 2.7 V to 5.5 V
- Low temperature coefficient: 35 ppm/°C
- Low power: I_{DD} = 6 µA max
- Wide operating temperature: –40°C to +125°C
- Evaluation board available

APPLICATIONS

- Systems calibrations
- Electronics level settings
- Mechanical Trimmers® replacement in new designs
- Permanent factory PCB setting
- Transducer adjustment of pressure, temperature, position, chemical, and optical sensors
- RF amplifier biasing
- Automotive electronics adjustment
- Gain control and offset adjustment

FUNCTIONAL BLOCK DIAGRAMS

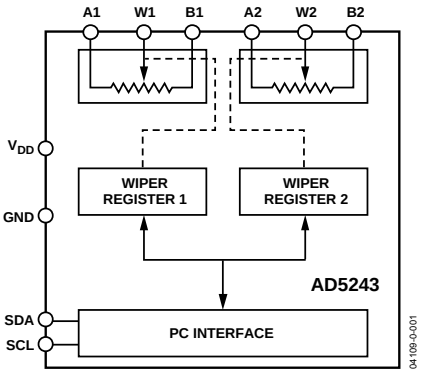

Figure 1. AD5243

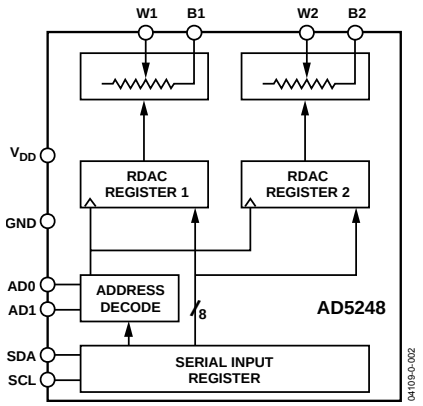

Figure 2. AD5248

GENERAL DESCRIPTION

The AD5243 and AD5248 provide a compact 3 mm × 4.9 mm packaged solution for dual 256-position adjustment applications. These devices perform the same electronic adjustment function as a 3-terminal mechanical potentiometer (AD5243) or a 2-terminal variable resistor (AD5248). Available in four different end-to-end resistance values (2.5 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ), these low temperature coefficient devices are ideal for high accuracy and stability variable resistance adjustments. The wiper settings are controllable through the I²C compatible digital interface. The AD5248 has extra package address decode pins AD0 and AD1, allowing multiple parts to share the same I²C 2-wire bus on a PCB. The resistance between the wiper and either endpoint of the fixed resistor varies linearly with respect to the digital code transferred into the RDAC latch.[1]

Operating from a 2.7 V to 5.5 V power supply and consuming less than 6 µA allows for usage in portable battery-operated applications.

For applications that program the AD5243/AD5258 at the factory, Analog Devices offers device programming software running on Windows® NT/2000/XP operating systems. This software effectively replaces any external I²C controllers, which in turn enhances users' systems time-to-market. An AD5243/AD5248 evaluation kit and software are available. The kit includes a cable and instruction manual.

[1]The terms *digital potentiometer*, *VR*, and *RDAC* are used interchangeably.

Rev. 0

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TABLE OF CONTENTS

REVISION HISTORY

Revision 0: Initial Version

ELECTRICAL CHARACTERISTICS—2.5 kΩ VERSION

V_{DD} = 5 V ± 10%, or 3 V ± 10%; $V_A = +V_{DD}$; V_B = 0 V; −40°C < T_A < +125°C; unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect	−2	±0.1	+2	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	−6	±0.75	+6	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = 25°C	−20		+55	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T$	$V_{AB} = V_{DD}$, wiper = no connect		35		ppm/°C
R_{WB} (Wiper Resistance)	R_{WB}	Code = 0x00, V_{DD} = 5 V		160	200	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (Specifications Apply to All VRs)						
Differential Nonlinearity[4]	DNL		−1.5	±0.1	+1.5	LSB
Integral Nonlinearity	INL		−2	±0.6	+2	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T$	Code = 0x80		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0xFF	−10	−2.5	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	2	10	LSB
RESISTOR TERMINALS						
Voltage Range[5]	V_A, V_B, V_W		GND		V_{DD}	V
Capacitance[6] A, B	C_A, C_B	f = 1 MHz, measured to GND, Code = 0x80		45		pF
Capacitance[6] W	C_W	f = 1 MHz, measured to GND, Code = 0x80		60		pF
Shutdown Supply Current[7]	I_{A_SD}	V_{DD} = 5.5 V		0.01	1	µA
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_{DD}/2$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = 5 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = 5 V			0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		3.5	6	µA
Power Dissipation[8]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			30	µW
Power Supply Sensitivity	PSS	V_{DD} = 5 V ± 10%, Code = midscale		±0.02	±0.08	%/%
DYNAMIC CHARACTERISTICS [9]						
Bandwidth −3 dB	BW_2.5 K	Code = 0x80		4.8		MHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz		0.1		%
V_W Settling Time	t_S	V_A = 5 V, V_B = 0 V, ±1 LSB error band		1		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 1.25 kΩ, R_S = 0		3.2		nV/√Hz

See notes at end of section.

ELECTRICAL CHARACTERISTICS—10 kΩ, 50 kΩ, 100 kΩ VERSIONS

V_{DD} = 5 V ± 10%, or 3 V ± 10%; $V_A = V_{DD}$; V_B = 0 V; −40°C < T_A < 125°C; unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect	−1	±0.1	+1	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	−2.5	±0.25	+2.5	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = 25°C	−20		+20	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T$	$V_{AB} = V_{DD}$, wiper = no connect		35		ppm/°C
R_{WB} (Wiper Resistance)	R_{WB}	Code = 0x00, V_{DD} =5 V		160	200	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (Specifications Apply to All VRs)						
Differential Nonlinearity[4]	DNL		−1	±0.1	+1	LSB
Integral Nonlinearity[4]	INL		−1	±0.3	+1	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T$	Code = 0x80		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0xFF	−2.5	−1	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	1	2.5	LSB
RESISTOR TERMINALS						
Voltage Range[5]	V_A, V_B, V_W		GND		V_{DD}	V
Capacitance[6] A, B	C_A, C_B	f = 1 MHz, measured to GND, Code = 0x80		45		pF
Capacitance[6] W	C_W	f = 1 MHz, measured to GND, Code = 0x80		60		pF
Shutdown Supply Current[7]	I_{A_SD}	V_{DD} = 5.5 V		0.01	1	µA
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_{DD}/2$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = 5 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = 5 V			0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		3.5	6	µA
Power Dissipation	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			30	µW
Power Supply Sensitivity	PSS	V_{DD} = 5 V ± 10%, Code = midscale		±0.02	±0.08	%/%
DYNAMIC CHARACTERISTICS						
Bandwidth −3 dB	BW	R_{AB} = 10 kΩ/50 kΩ/100 kΩ, Code = 0x80		600/100/40		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz, R_{AB} = 10 kΩ		0.1		%
V_W Settling Time (10 kΩ/50 kΩ/100 kΩ)	t_S	V_A = 5 V, V_B = 0 V, ±1 LSB error band		2		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 5 kΩ, R_S = 0		9		nV/√Hz

See notes at end of section.

TIMING CHARACTERISTICS—ALL VERSIONS

V_{DD} = 5V ± 10%, or 3V ± 10%; $V_A = V_{DD}$; V_B = 0 V; −40°C < T_A < +125°C; unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
I²C INTERFACE TIMING CHARACTERISTICS[10] (Specifications Apply to All Parts)						
SCL Clock Frequency	f_{SCL}		0		400	kHz
t_{BUF} Bus Free Time between STOP and START	t_1		1.3			µs
$t_{HD;STA}$ Hold Time (Repeated START)	t_2	After this period, the first clock pulse is generated.	0.6			µs
t_{LOW} Low Period of SCL Clock	t_3		1.3			µs
t_{HIGH} High Period of SCL Clock	t_4		0.6			µs
$t_{SU;STA}$ Setup Time for Repeated START Condition	t_5		0.6			µs
$t_{HD;DAT}$ Data Hold Time[11]	t_6				0.9	µs
$t_{SU;DAT}$ Data Setup Time	t_7		100			ns
t_F Fall Time of Both SDA and SCL Signals	t_8				300	ns
t_R Rise Time of Both SDA and SCL Signals	t_9				300	ns
$t_{SU;STO}$ Setup Time for STOP Condition	t_{10}		0.6			µs

See notes at end of section.

NOTES

[1] Typical specifications represent average readings at 25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
[3] $V_{AB} = V_{DD}$, wiper (VW) = no connect.
[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor terminals A, B, W have no limitations on polarity with respect to each other.
[6] Guaranteed by design and not subject to production test.
[7] Measured at the A terminal. The A terminal is open circuited in shutdown mode.
[8] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.
[9] All dynamic characteristics use V_{DD} = 5 V.
[10] See timing diagrams for locations of measured values.
[11] The maximum $t_{HD;DAT}$ must be met only if the device does not stretch the low period (t_{LOW}) of the SCL signal.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Value
V_{DD} to GND	–0.3 V to +7 V
V_A, V_B, V_W to GND	V_{DD}
Terminal Current, Ax to Bx, Ax to Wx, Bx to Wx[1]	
Pulsed	±20 mA
Continuous	±5 mA
Digital Inputs and Output Voltage to GND	0 V to 7 V
Operating Temperature Range	–40°C to +125°C
Maximum Junction Temperature (T_{JMAX})	150°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Thermal Resistance[2] θ_{JA}: MSOP-10	230°C/W

[1]Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

[2]Package power dissipation = $(T_{JMAX} - T_A)/\theta_{JA}$.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

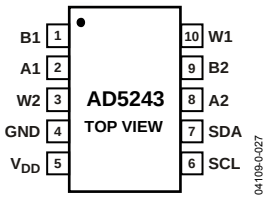

Figure 3. AD5243 Pin Configuration

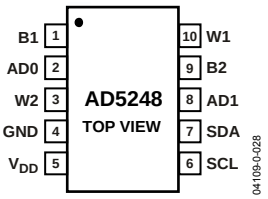

Figure 4. AD5248 Pin Configuration

Table 5. AD5243 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	B1	B1 Terminal.
2	A1	A1 Terminal.
3	W2	W2 Terminal.
4	GND	Digital Ground.
5	V_{DD}	Positive Power Supply.
6	SCL	Serial Clock Input. Positive edge triggered.
7	SDA	Serial Data Input/Output.
8	A2	A2 Terminal.
9	B2	B2 Terminal.
10	W1	W1 Terminal.

Table 6. AD5248 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	B1	B1 Terminal.
2	AD0	Programmable Address Bit 0 for Multiple Package Decoding.
3	W2	W2 Terminal.
4	GND	Digital Ground.
5	V_{DD}	Positive Power Supply.
6	SCL	Serial Clock Input. Positive edge triggered.
7	SDA	Serial Data Input/Output.
8	AD1	Programmable Address Bit 1 for Multiple Package Decoding.
9	B2	B2 Terminal.
10	W1	W1 Terminal.

TYPICAL PERFORMANCE CHARACTERISTICS

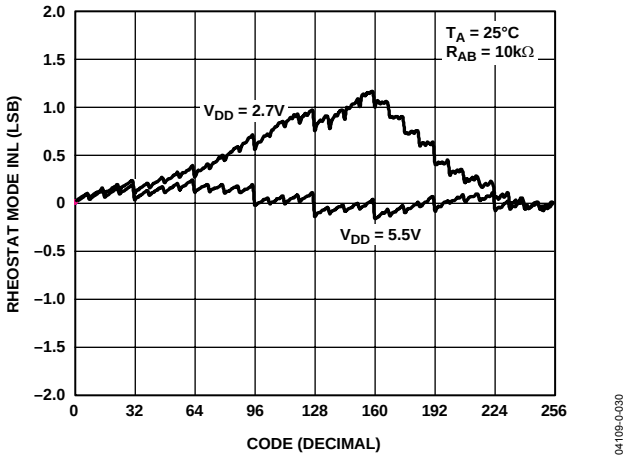

Figure 5. R-INL vs. Code vs. Supply Voltages

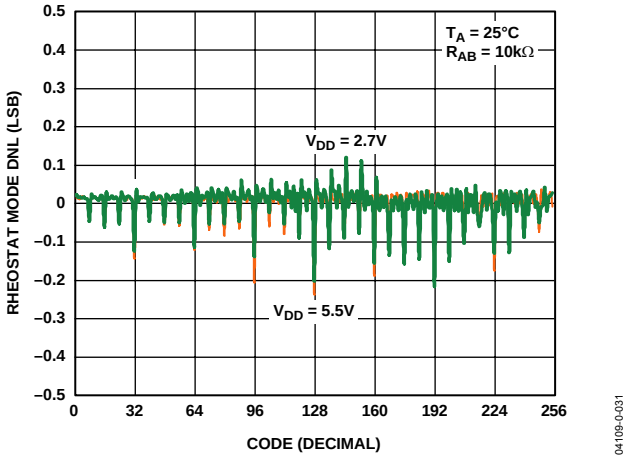

Figure 6. R-DNL vs. Code vs. Supply Voltages

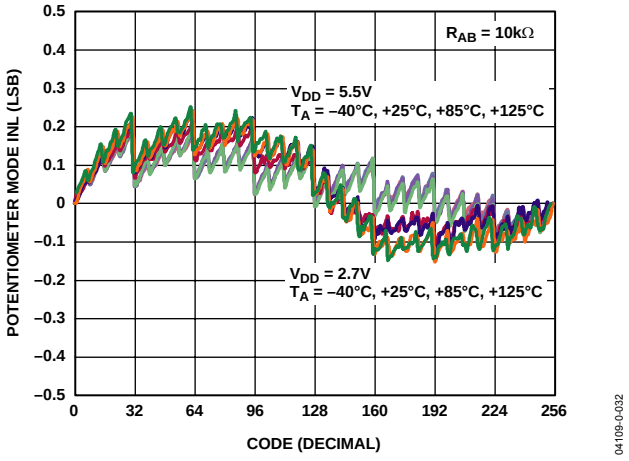

Figure 7. INL vs. Code vs. Temperature

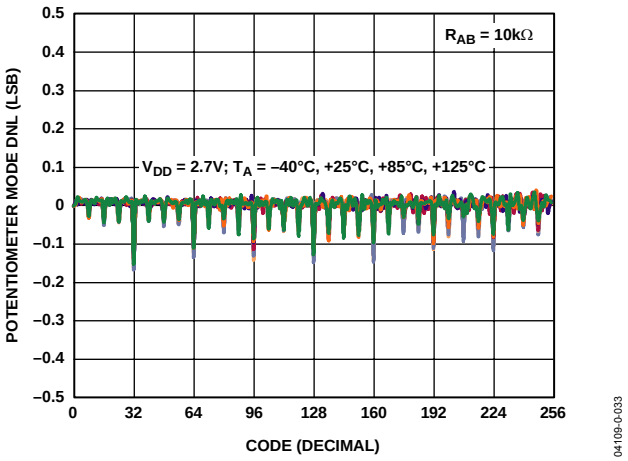

Figure 8. DNL vs. Code vs. Temperature

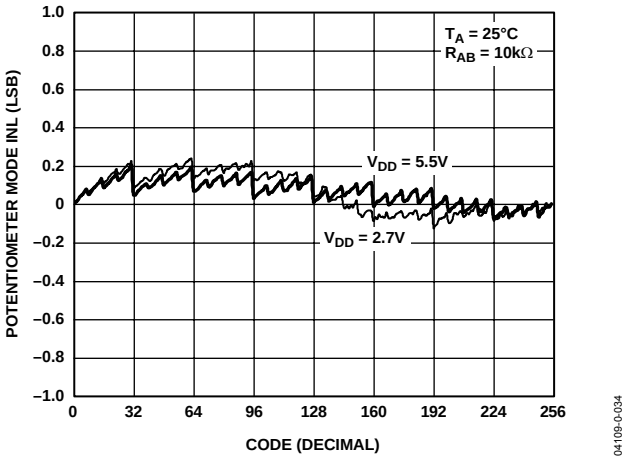

Figure 9. INL vs. Code vs. Supply Voltages

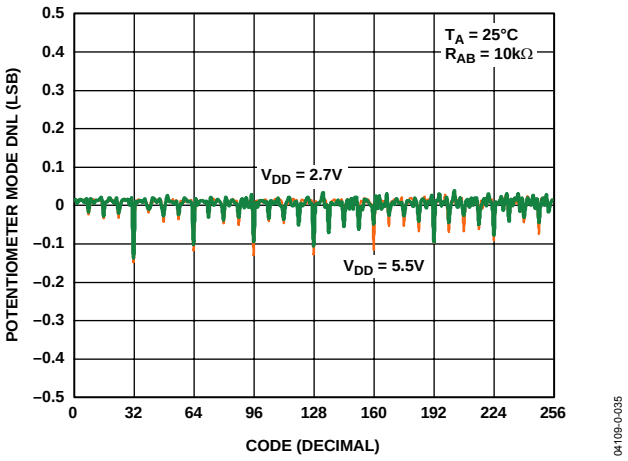

Figure 10. DNL vs. Code vs. Supply Voltages

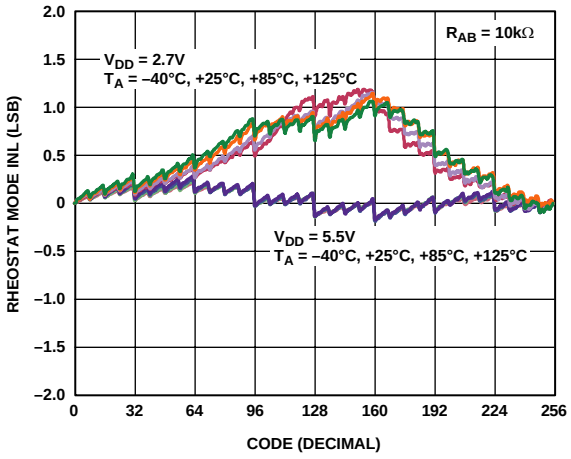

Figure 11. R-INL vs. Code vs. Temperature

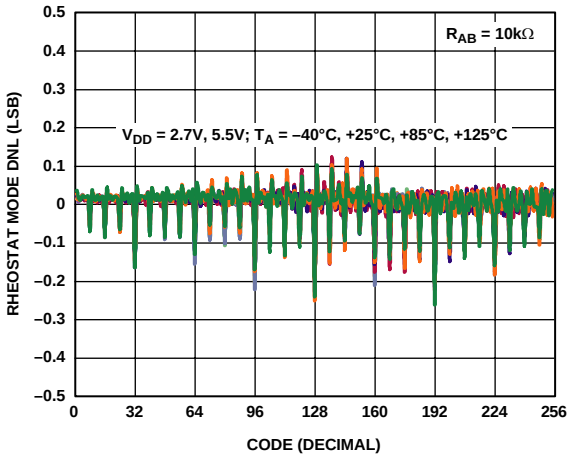

Figure 12. R-DNL vs. Code vs. Temperature

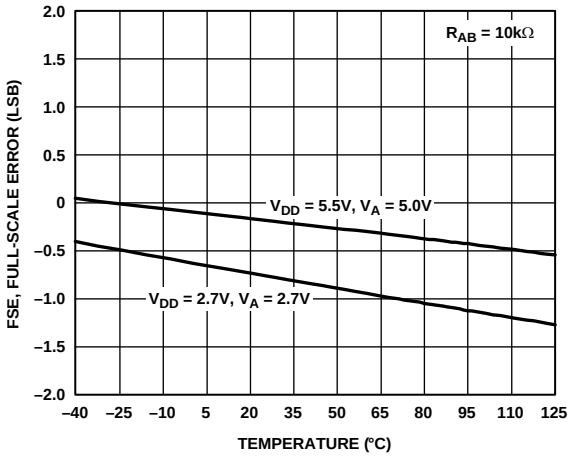

Figure 13. Full-Scale Error vs. Temperature

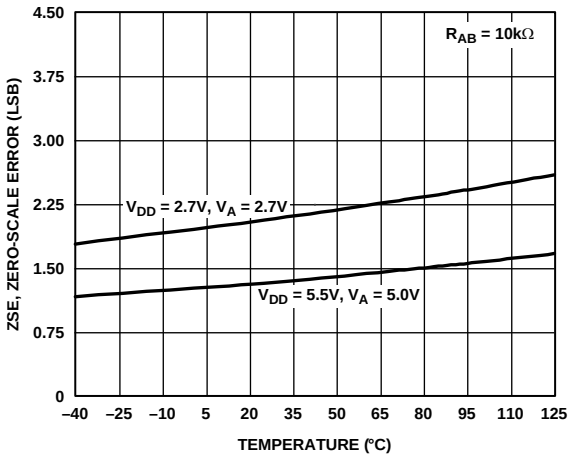

Figure 14. Zero-Scale Error vs. Temperature

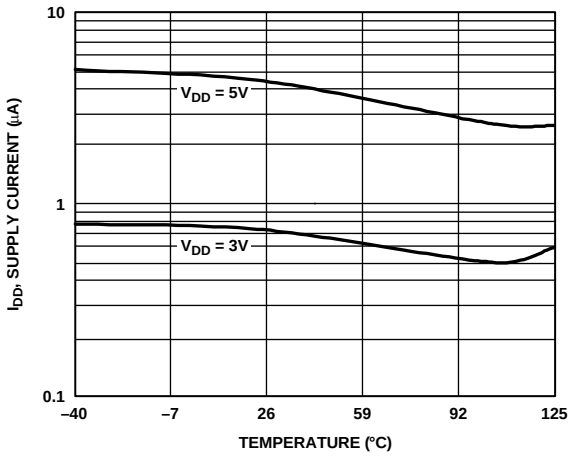

Figure 15. Supply Current vs. Temperature

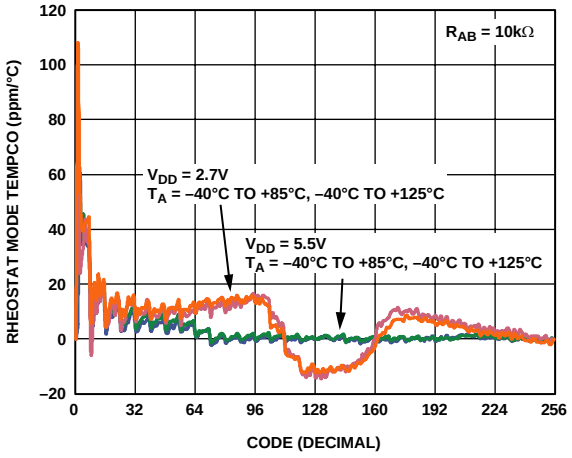

Figure 16. Rheostat Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code

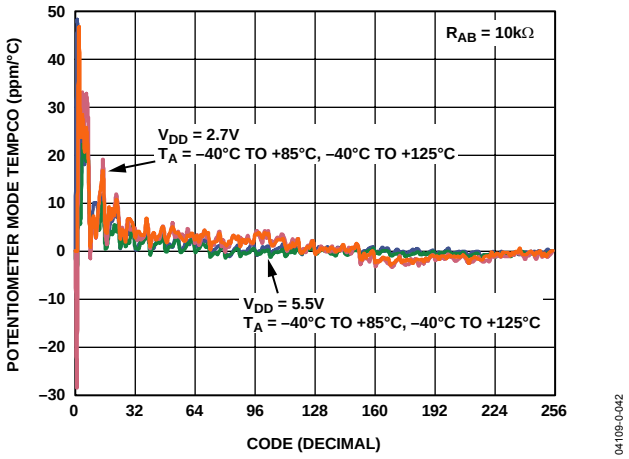

Figure 17. Potentiometer Mode Tempco $\Delta V_{WB}/\Delta T$ vs. Code

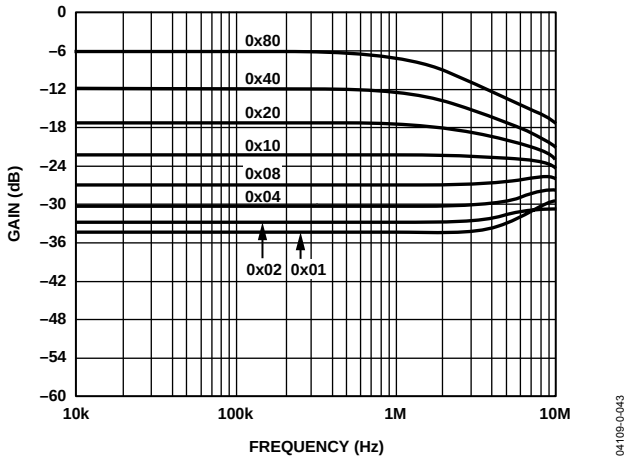

Figure 18. Gain vs. Frequency vs. Code, R_{AB} = 2.5 kΩ

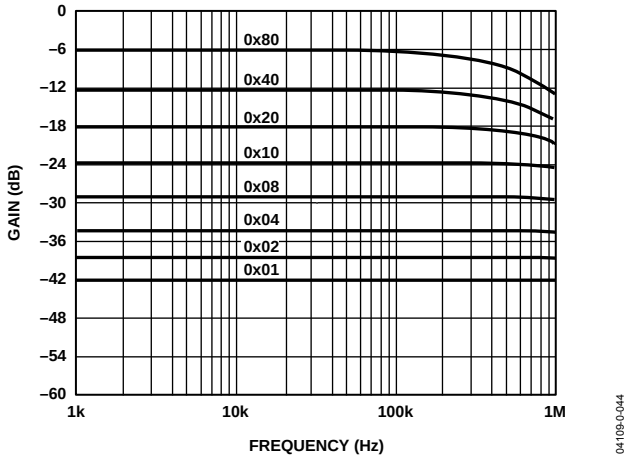

Figure 19. Gain vs. Frequency vs. Code, R_{AB} = 10 kΩ

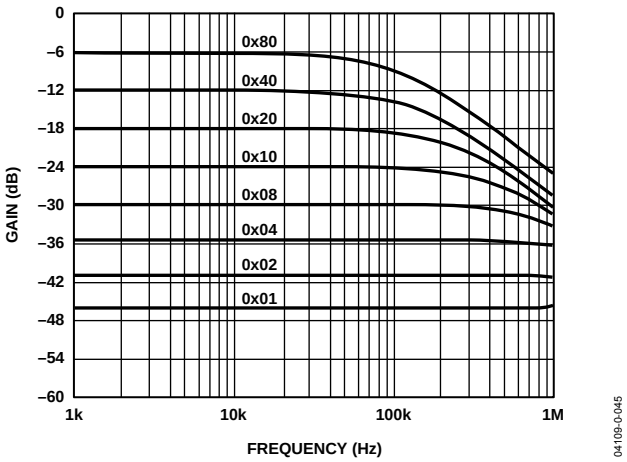

Figure 20. Gain vs. Frequency vs. Code, R_{AB} = 50 kΩ

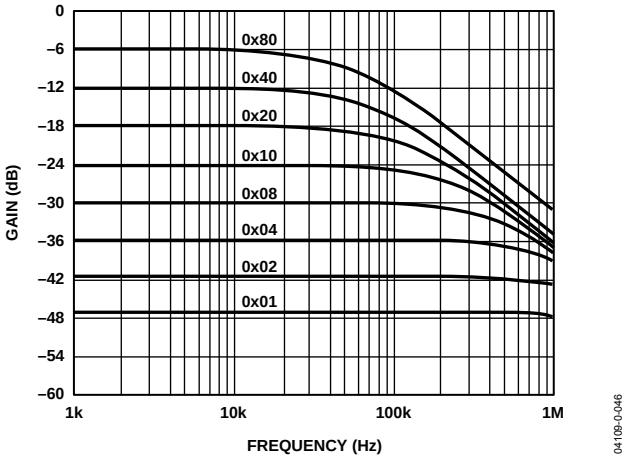

Figure 21. Gain vs. Frequency vs. Code, R_{AB} = 100 kΩ

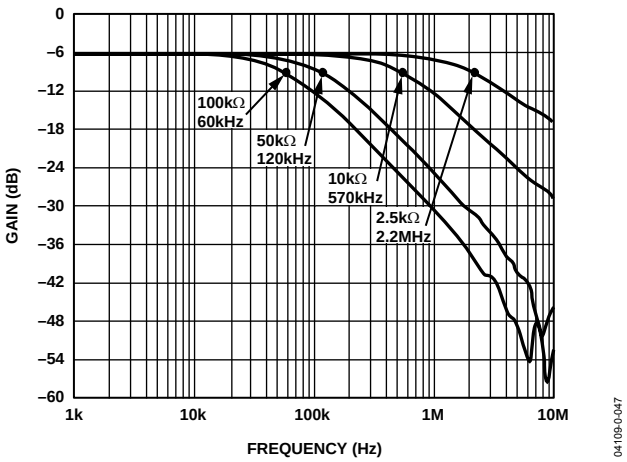

Figure 22. –3 dB Bandwidth @ Code = 0x80

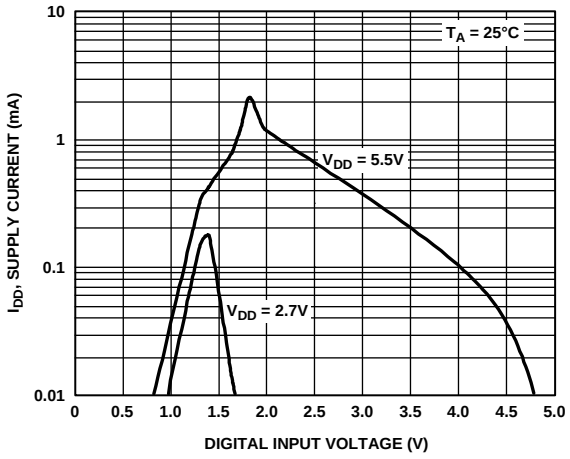

Figure 23. I_{DD} vs. Input Voltage

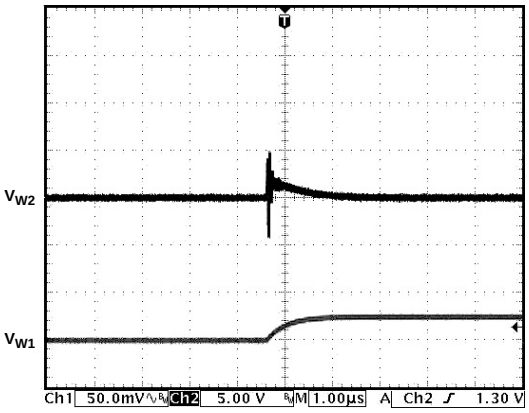

Figure 26. Analog Crosstalk

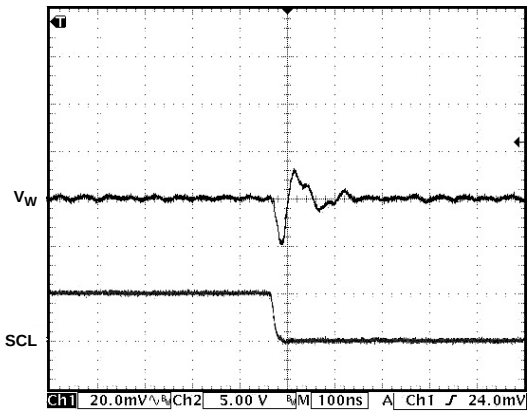

Figure 24. Digital Feedthrough

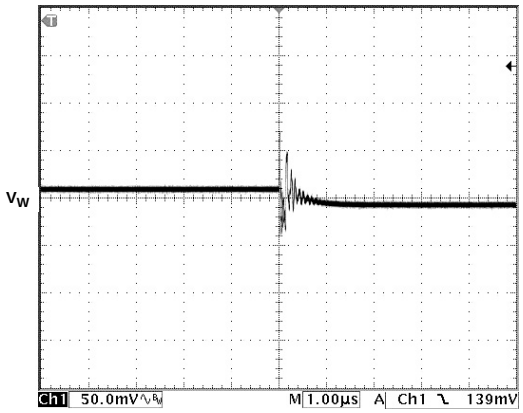

Figure 27. Midscale Glitch, Code 0x80 to 0x7F

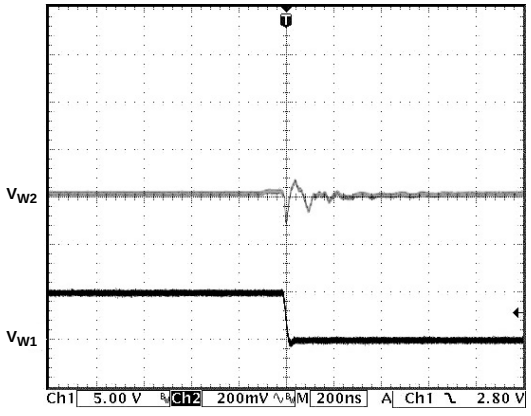

Figure 25. Digital Crosstalk

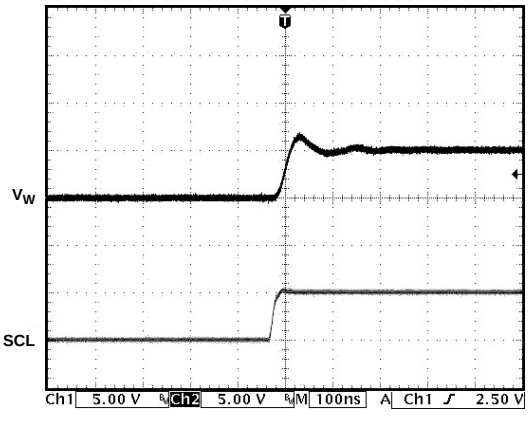

Figure 28. Large Signal Settling Time

TEST CIRCUITS

Figure 29 through Figure 35 illustrate the test circuits that define the test conditions used in the product specification tables.

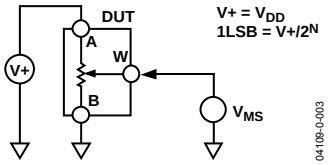

Figure 29. Test Circuit for Potentiometer Divider Nonlinearity Error (INL, DNL)

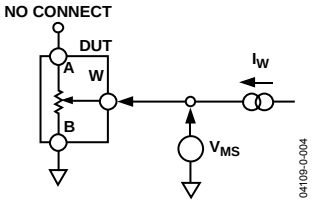

Figure 30. Test Circuit for Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

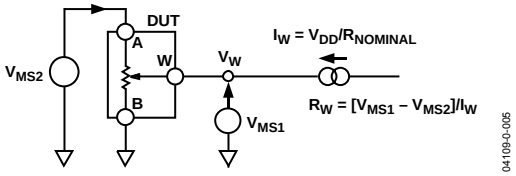

Figure 31. Test Circuit for Wiper Resistance

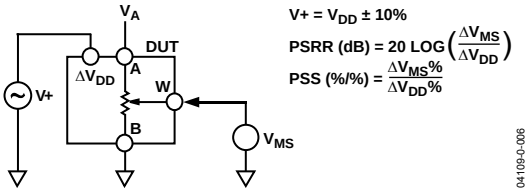

Figure 32. Test Circuit for Power Supply Sensitivity(PSS, PSSR)

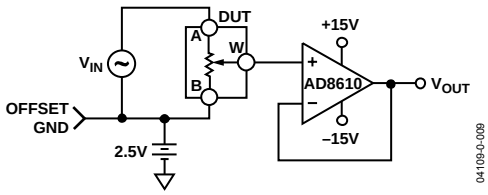

Figure 33. Test Circuit for Gain vs. Frequency

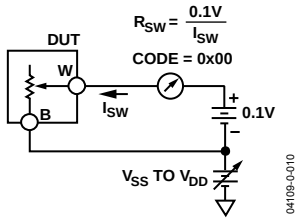

Figure 34. Test Circuit for Incremental On Resistance

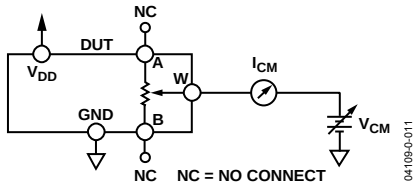

Figure 35. Test Circuit for Common-Mode Leakage Current

THEORY OF OPERATION

The AD5243/AD5248 are 256-position digitally controlled variable resistor (VR) devices.

An internal power-on preset places the wiper at midscale during power-on, which simplifies the fault condition recovery at power-up.

PROGRAMMING THE VARIABLE RESISTOR AND VOLTAGE

Rheostat Operation

The nominal resistance of the RDAC between Terminals A and B is available in 2.5 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ. The nominal resistance (R_{AB}) of the VR has 256 contact points accessed by the wiper terminal, plus the B terminal contact. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible settings.

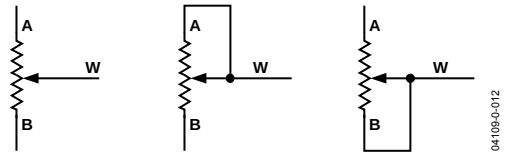

Figure 36. Rheostat Mode Configuration

Assuming that a 10 kΩ part is used, the wiper's first connection starts at the B terminal for data 0x00. Because there is a 50 Ω wiper contact resistance, such a connection yields a minimum of 100 Ω (2 × 50 Ω) resistance between Terminals W and B. The second connection is the first tap point, which corresponds to 139 Ω ($R_{WB} = R_{AB}/256 + 2 \times R_W$ = 39 Ω + 2 × 50 Ω) for data 0x01. The third connection is the next tap point, representing 178 Ω (2 × 39 Ω + 2 × 50 Ω) for data 0x02, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10,100 Ω (R_{AB} + 2 × R_W).

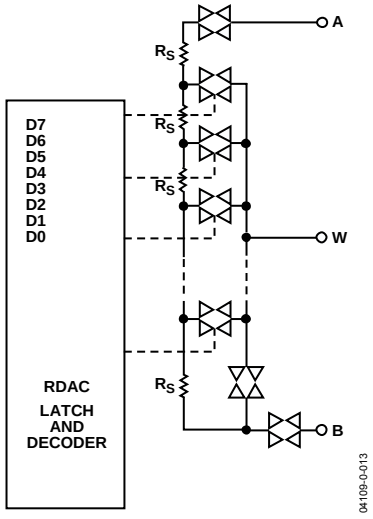

Figure 37. AD5243 Equivalent RDAC Circuit

The general equation determining the digitally programmed output resistance between W and B is

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + 2 \times R_W \quad (1)$$

where:

D is the decimal equivalent of the binary code loaded in the 8-bit RDAC register.
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance contributed by the on resistance of the internal switch.

In summary, if R_{AB} = 10 kΩ and the A terminal is open circuited, the following output resistance R_{WB} is set for the indicated RDAC latch codes.

Table 7. Codes and Corresponding R_{WB} Resistance

D (Dec)	R_{WB} (Ω)	Output State
255	9,961	Full scale (R_{AB} − 1 LSB + R_W)
128	5,060	Midscale
1	139	1 LSB
0	100	Zero scale (wiper contact resistance)

Note that, in the zero-scale condition, a finite wiper resistance of 100 Ω is present. Care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the Wiper W and Terminal A also produces a digitally controlled complementary resistance, R_{WA}. When these terminals are used, the B terminal can be opened. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{256} \times R_{AB} + 2 \times R_W \quad (2)$$

For R_{AB} = 10 kΩ and the B terminal open circuited, the following output resistance R_{WA} is set for the indicated RDAC latch codes.

Table 8. Codes and Corresponding R_{WA} Resistance

D (Dec)	R_{WA} (Ω)	Output State
255	139	Full scale
128	5,060	Midscale
1	9,961	1 LSB
0	10,060	Zero scale

Typical device-to-device matching is process lot dependent and may vary by up to ±30%. Because the resistance element is processed in thin film technology, the change in R_{AB} with temperature has a very low 35 ppm/°C temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper-to-B and wiper-to-A proportional to the input voltage at A to B. Unlike the polarity of V_{DD} to GND, which must be positive, voltage across A to B, W to A, and W to B can be at either polarity.

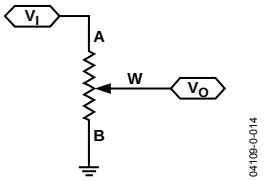

Figure 38. Potentiometer Mode Configuration

If ignoring the effect of the wiper resistance for approximation, connecting the A terminal to 5 V and the B terminal to ground produces an output voltage at the wiper-to-B starting at 0 V up to 1 LSB less than 5 V. Each LSB of voltage is equal to the voltage applied across terminal AB divided by the 256 positions of the potentiometer divider. The general equation defining the output voltage at V_W with respect to ground for any valid input voltage applied to terminals A and B is

$$V_W(D) = \frac{D}{256}V_A + \frac{256 - D}{256}V_B \quad (3)$$

A more accurate calculation, which includes the effect of wiper resistance, V_W, is

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}}V_A + \frac{R_{WA}(D)}{R_{AB}}V_B \quad (4)$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation overtemperature. Unlike the rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors R_{WA} and R_{WB} and not the absolute values. Therefore, the temperature drift reduces to 15 ppm/°C.

ESD PROTECTION

All digital inputs are protected with a series of input resistors and parallel Zener ESD structures, shown in Figure 39 and Figure 40. This applies to the digital input pins SDA, SCL, AD0, and AD1 (AD5248 only).

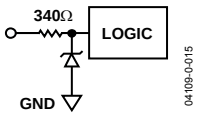

Figure 39. ESD Protection of Digital Pins

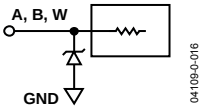

Figure 40. ESD Protection of Resistor Terminals

TERMINAL VOLTAGE OPERATING RANGE

The AD5243/AD5248 V_{DD} and GND power supply defines the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on Terminals A, B, and W that exceed V_{DD} or GND are clamped by the internal forward biased diodes (see Figure 41).

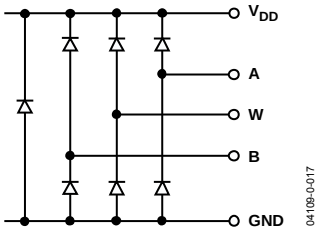

Figure 41. Maximum Terminal Voltages Set by V_{DD} and GND

POWER-UP SEQUENCE

Because the ESD protection diodes limit the voltage compliance at Terminals A, B, and W (see Figure 41), it is important to power V_{DD}/GND before applying any voltage to Terminals A, B, and W; otherwise, the diode is forward biased such that V_{DD} is powered unintentionally and may affect the rest of the user's circuit. The ideal power-up sequence is in the following order: GND, V_{DD}, digital inputs, and then V_A, V_B, and V_W. The relative order of powering V_A, V_B, V_W, and the digital inputs is not important as long as they are powered after V_{DD}/GND.

LAYOUT AND POWER SUPPLY BYPASSING

It is good practice to employ compact, minimum lead length layout design. The leads to the inputs should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with disk or chip ceramic capacitors of 0.01 µF to 0.1 µF. Low ESR 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at the supplies to minimize any transient disturbance and low frequency ripple (see Figure 42). Note that the digital ground should also be joined remotely to the analog ground at one point to minimize the ground bounce.

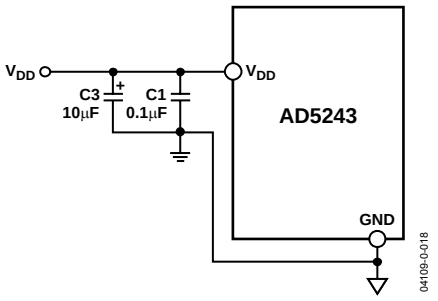

Figure 42. Power Supply Bypassing

CONSTANT BIAS TO RETAIN RESISTANCE SETTING

For users who desire nonvolatility but cannot justify the additional cost for the EEMEM, the AD5243/AD5248 may be considered as low cost alternatives by maintaining a constant bias to retain the wiper setting. The AD5243/AD5248 are designed specifically with low power in mind, which allows low power consumption even in battery-operated systems. The graph in Figure 43 demonstrates the power consumption from a 3.4 V 450 mAhr Li-Ion cell phone battery, which is connected to the AD5243/AD5248. The measurement over time shows that the device draws approximately 1.3 µA and consumes negligible power. Over a course of 30 days, the battery is depleted by less than 2%, the majority of which is due to the intrinsic leakage current of the battery itself.

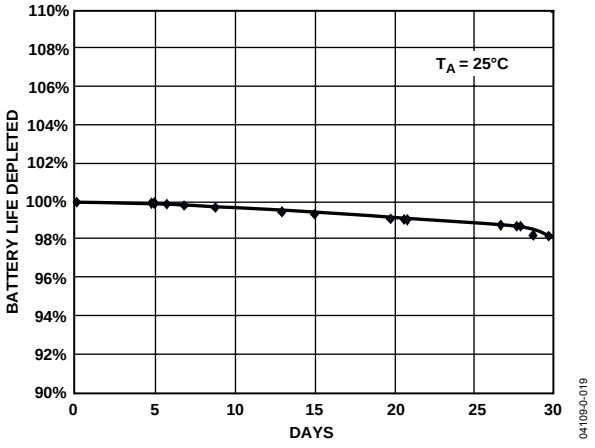

Figure 43. Battery Operating Life Depletion

This demonstrates that constantly biasing the potentiometer is not an impractical approach. Most portable devices do not require the removal of batteries for the purpose of charging. Although the resistance setting of the AD5243/AD5248 is lost when the battery needs replacement, such events occur rather infrequently such that this inconvenience is justified by the lower cost and smaller size offered by the AD5243/AD5248. If and when total power is lost, the user should be provided with a means to adjust the setting accordingly.

EVALUATION BOARD

An evaluation board, along with all necessary software, is available to program the AD5243/AD5248 from any PC running Windows 98/2000/XP. The graphical user interface, as shown in Figure 44, is straightforward and easy to use. More detailed information is available in the user manual, which comes with the board.

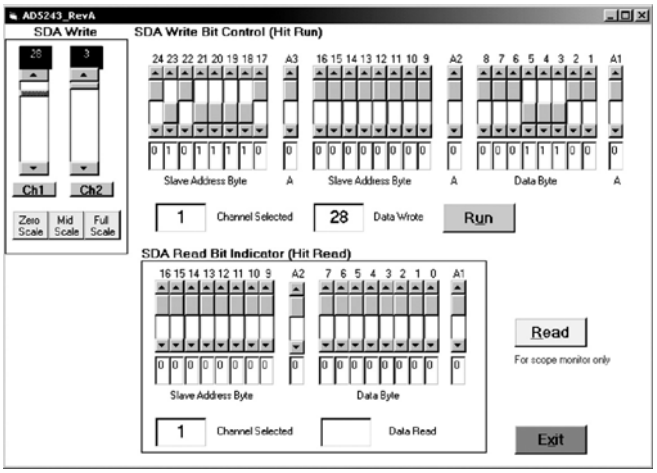

Figure 44. AD5243 Evaluation Board Software

The AD5243/AD5248 start at midscale upon power-up. To increment or decrement the resistance, the user may simply move the scrollbars on the left. To write any specific value, the user should use the bit pattern in the upper screen and press the Run button. The format of writing data to the device is shown in Table 9. To read the data out from the device, the user can simply press the Read button. The format of the read bits is shown in Table 10.

I²C INTERFACE

I²C COMPATIBLE 2-WIRE SERIAL BUS

The 2-wire I²C serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, which is when a high-to-low transition on the SDA line occurs while SCL is high (see Figure 46). The following byte is the slave address byte, which consists of the slave address followed by an R/$\overline{W}$ bit (this bit determines whether data is read from or written to the slave device). The AD5243 has a fixed slave address byte, while the AD5248 has two configurable address bits AD0 and AD1 (see Table 9).

   The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register. If the R/$\overline{W}$ bit is high, the master reads from the slave device. On the other hand, if the R/$\overline{W}$ bit is low, the master writes to the slave device.

2. In the write mode, the second byte is the instruction byte. The first bit (MSB) of the instruction byte is the RDAC subaddress select bit. A Logic Low selects Channel 1 and a Logic High selects Channel 2.

   The second MSB, SD, is a shutdown bit. A logic high causes an open circuit at Terminal A while shorting the wiper to Terminal B. This operation yields almost 0 Ω in rheostat mode or 0 V in potentiometer mode. It is important to note that the shutdown operation does not disturb the contents of the register. When brought out of shutdown, the previous setting is applied to the RDAC. Also, during shutdown, new settings can be programmed. When the part is returned from shutdown, the corresponding VR setting is applied to the RDAC.

   The remainder of the bits in the instruction byte are don't care bits (see Table 9).

   After acknowledging the instruction byte, the last byte in write mode is the data byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 46 and Figure 47).

3. In the read mode, the data byte follows immediately after the acknowledgment of the slave address byte. Data is transmitted over the serial bus in sequences of nine clock pulses (a slight difference with the write mode, eight data bits are followed by an acknowledge bit). Similarly, the transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 48 and Figure 49).

   Note that the channel of interest is the one that is previously selected in the write mode. In the case where users need to read the RDAC values of both channels, they need to program the first channel in the write mode and then change to the read mode to read the first channel value. After that, they need to change back to the write mode with the second channel selected and read the second channel value in the read mode again. It is not necessary for users to issue the Frame 3 data byte in the write mode for subsequent readback operation. Users should refer to Figure 48 and Figure 49 for the programming format.

4. After all data bits have been read or written, a STOP condition is established by the master. A STOP condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master pulls the SDA line high during the tenth clock pulse to establish a STOP condition (see Figure 46 and Figure 47). In read mode, the master issues a no acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the tenth clock pulse, which goes high to establish a STOP condition (see Figure 48 and Figure 49).

   A repeated write function gives the user flexibility to update the RDAC output a number of times after addressing and instructing the part only once. For example, after the RDAC has acknowledged its slave address and instruction bytes in the write mode, the RDAC output updates on each successive byte. If different instructions are needed, the write/read mode has to start again with a new slave address, instruction, and data byte. Similarly, a repeated read function of the RDAC is also allowed.

Table 9. Write Mode

AD5243

S	0	1	0	1	1	1	1	W	A	A0	SD	X	X	X	X	X	X	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Instruction Byte									Data Byte									

AD5248

S	0	1	0	1	1	AD1	AD0	W	A	A0	SD	X	X	X	X	X	X	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Instruction Byte									Data Byte									

Table 10. Read Mode

AD5243

S	0	1	0	1	1	1	1	R	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Data Byte									

AD5248

S	0	1	0	1	1	AD1	AD0	R	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Data Byte									

LEGEND	
S = Start condition.	R = Read.
P = Stop condition.	A0 = RDAC subaddress select bit.
A = Acknowledge.	SD = Shutdown connects wiper to B terminal and open circuits A terminal. It does not change contents of wiper register.
X = Don't care.	
W = Write.	
AD0, AD1 = Package pin programmable address bits.	D7, D6, D5, D4, D3, D2, D1, D0 = Data bits.

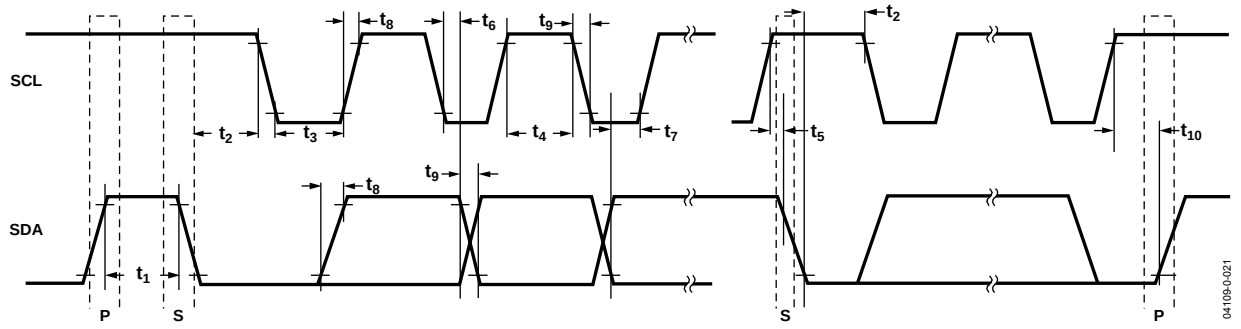

Figure 45. I²C Interface Detailed Timing Diagram

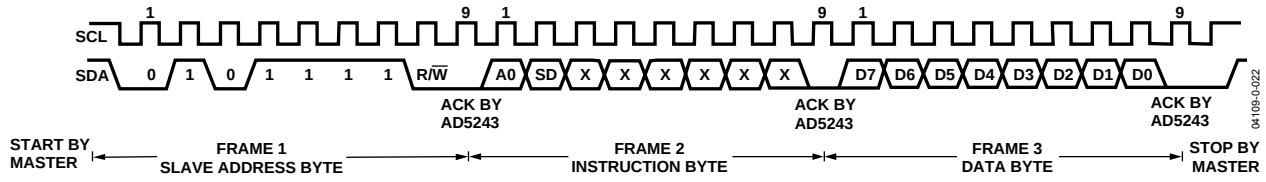

Figure 46. Writing to the RDAC Register—AD5243

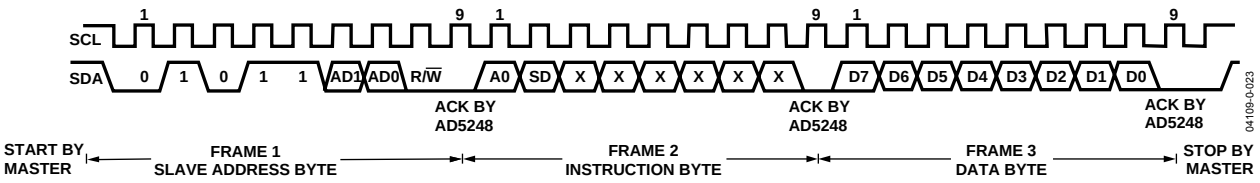

Figure 47. Writing to the RDAC Register—AD5248

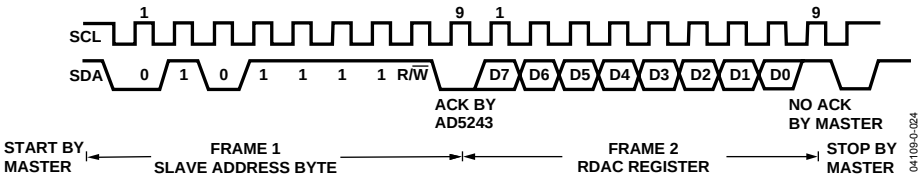

Figure 48. Reading Data from a Previously Selected RDAC Register in Write Mode—AD5243

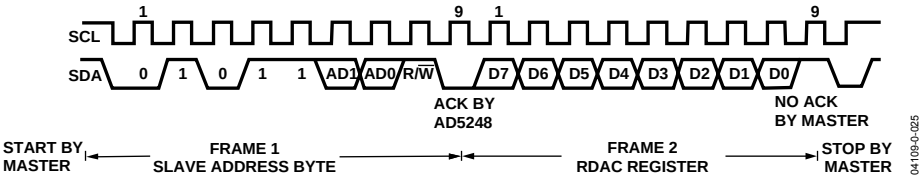

Figure 49. Reading Data from a Previously Selected RDAC Register in Write Mode—AD5248

Multiple Devices on One Bus (Applies Only to AD5248)

Figure 50 shows four AD5248 devices on the same serial bus. Each has a different slave address, because the states of their AD0 and AD1 pins are different. This allows each device on the bus to be written to or read from independently. The master device output bus line drivers are open-drain pull-downs in a fully I²C compatible interface.

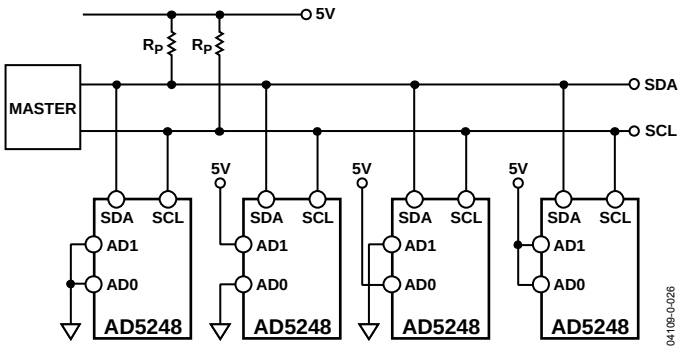

Figure 50. Multiple AD5248 Devices on One I²C Bus

OUTLINE DIMENSIONS

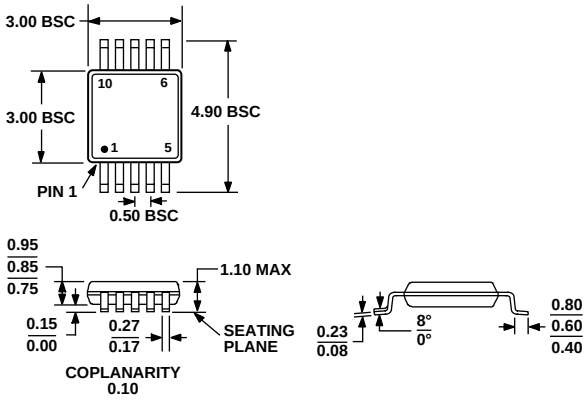

Figure 51. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	R_{AB}	Temperature	Package Description	Package Option	Branding
AD5243BRM2.5	2.5 kΩ	−40°C to +125°C	MSOP-10	RM-10	D0L
AD5243BRM2.5-RL7	2.5 kΩ	−40°C to +125°C	MSOP-10	RM-10	D0L
AD5243BRM10	10 kΩ	−40°C to +125°C	MSOP-10	RM-10	D0M
AD5243BRM10-RL7	10 kΩ	−40°C to +125°C	MSOP-10	RM-10	D0M
AD5243BRM50	50 kΩ	−40°C to +125°C	MSOP-10	RM-10	D0N
AD5243BRM50-RL7	50 kΩ	−40°C to +125°C	MSOP-10	RM-10	D0N
AD5243BRM100	100 kΩ	−40°C to +125°C	MSOP-10	RM-10	D0P
AD5243BRM100-RL7	100 kΩ	−40°C to +125°C	MSOP-10	RM-10	D0P
AD5243EVAL	See Note 1		Evaluation Board		
AD5248BRM2.5	2.5 kΩ	−40°C to +125°C	MSOP-10	RM-10	D1F
AD5248BRM2.5-RL7	2.5 kΩ	−40°C to +125°C	MSOP-10	RM-10	D1F
AD5248BRM10	10 kΩ	−40°C to +125°C	MSOP-10	RM-10	D1G
AD5248BRM10-RL7	10 kΩ	−40°C to +125°C	MSOP-10	RM-10	D1G
AD5248BRM50	50 kΩ	−40°C to +125°C	MSOP-10	RM-10	D1H
AD5248BRM50-RL7	50 kΩ	−40°C to +125°C	MSOP-10	RM-10	D1H
AD5248BRM100	100 kΩ	−40°C to +125°C	MSOP-10	RM-10	D1J
AD5248BRM100-RL7	100 kΩ	−40°C to +125°C	MSOP-10	RM-10	D1J
AD5248EVAL	See Note 1		Evaluation Board		

[1]The evaluation board is shipped with the 10 kΩ R_{AB} resistor option; however, the board is compatible with all available resistor value options.

NOTES

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